8-GHz CMOS Quadrature VCO Using Transformer-Based LC Tank

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***Abstract*—A fully integrated quadrature VCO at 8 GHz is presented. The VCO is implemented using a transformer-based LC tank in 0.18 μm CMOS technology, in which two VCOs are coupled to generate I-Q signals. The VCO is realized employing the drain-gate transformer feedback configuration proposed here. This makes use of the quality factor enhancement in the resonator using a transformer and the deep switching-off technique by controlling gate bias. By turning off switching transistors of the differential VCO core deeply, the phase noise performance is improved more than 10 dB. The measured phase noise values are -110 and -117 dBc/ HZ at the offset frequencies of 600 kHz and 1 MHz respectively. The tuning range of 250 MHz is achieved with the control voltage from 0 to 1 V. The VCO draws 8 mA in two differential core circuits from 3 V supply. When the bias voltage goes down to 2.5 V, the phase noise decrease only 2 dB compared to that of 3 V bias. The VCO performances are compared with previously reported quadrature Si VCOs in $5 \sim 12$ GHz frequency range.**

***Index Terms*—$1/f$ noise, CMOS, deep switching, quadrature, transformer, VCO.**

I. Introduction

THE fully integrated CMOS VCO has been paid great attention due to its low cost and the integrability with other analog and digital circuits although Si substrate has higher loss than GaAs substrate. The disadvantage associated with substrate loss is being conquered by the evolution of the process and the circuit technologies. For a few years, low-GHz CMOS VCOs have shown better performances than GaAs VCOs thanks to improving low noise characteristics of active devices and quality factor of passive devices [1]. When the operating frequency of a VCO increases, however, there still remain several hurdles to be overcome. The main hindrance of a CMOS VCO is also, low quality factor of an inductor. Recently it is reported that a transformer-based LC resonator has higher quality factor than that of a single LC resonator, resulting in enhancement of the phase noise performance of a VCO [2]. Until now, most of transformer based CMOS VCOs are published below 6 GHz. Furthermore, the transformer-based quadrature CMOS VCO has been not much reported.

In this paper, a new transformer-based VCO configuration is presented abiding by I-Q quadrature generation at 8 GHz. This new configuration allows deep-turn-off state of switching transistors, which gives low phase noise characteristics. In order to design VCO with low phase noise performance, following design principles are applied:

1) reduction of the noise of active device;
   - optimization of gate finger width and length in n-MOSFET;
   - deep-turn-off of switching pair when they are at off state;
2) maximization of tank voltage;
3) enhancement of quality factor: Transformer based LC-tank;
4) series current modulation for the quadrature coupling.

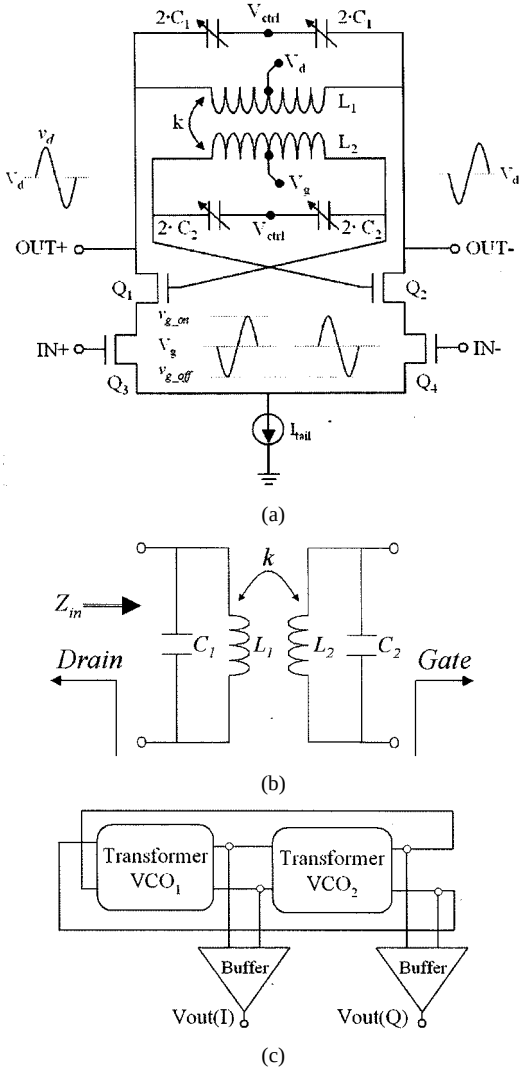

Fig. 1. (a) Schematic of the new transformer VCO, (b) transformer LC tank, and (c) quadrature generation.

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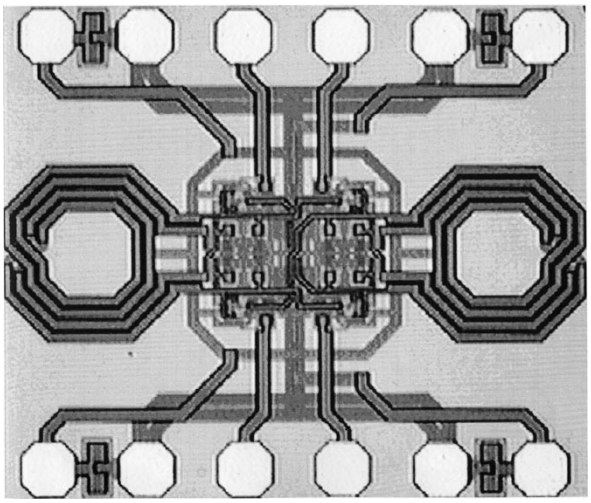

Fig. 2. Photograph of the fabricated quadrature VCO (900×750 μ m^2).

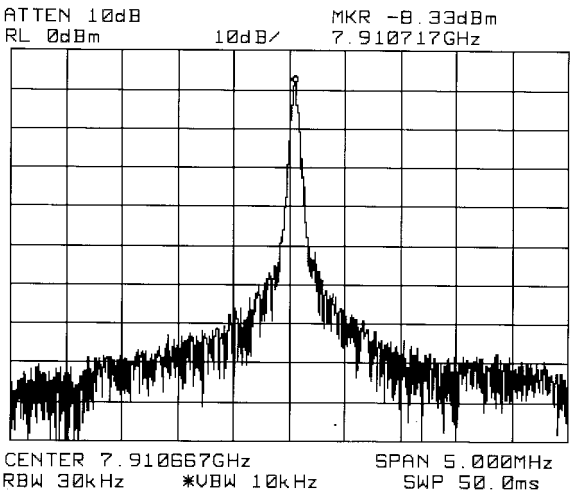

Fig. 3. Output spectrum of a quadrature VCO at the center frequency ($V_d = 3$ V, $V_g = 2$ V and $V_{ctrl} = 0.3$ V).

II. Transformer Feedback VCO Configuration

Fig. 1(a) shows a simplified circuit schematic of the proposed transformer based VCO. The tank voltage (v_d) is transferred to gate with the same phase through mutual inductance between primary coil (L_1) to secondary coil (L_2). DC bias level of the tank voltage is shifted from V_d in the drain to V_g in the gate. To make total phase shift of loop gain 0° and generate negative resistance for compensating the loss of LC tank, secondary coils are cross-connected with gate terminals. LC-resonator is composed of L_1 and C_1 in drain and L_2 and C_2 in the gate as shown Fig. 1(b). This transformer-based LC tank has better quality factor than a single LC tank. If $L = L_1 = L_2$ and $C = C_1 = C_2$ are assumed, the resonant frequency and the quality factor can be described by

$$f_0 = \frac{1}{2\pi\sqrt{L \cdot (1+k)C}},\ Q = (1+k)Q_0 \qquad (1)$$

where k is the coupling coefficient of a transformer and Q_0 is the quality factor of a single LC-resonator which is composed of L and $(1 + k)$ C or $(1 + k)$ L and C. The transformer has inductances of 2 nH (L_1) in the primary coil and 1.6 nH (L_2) in the secondary coil. And the quality factor is about 7.5 when the differential signal is applied. The coupling coefficient (k) is 0.7. Inversion type MOS varactors are used to tune oscillation frequency. To block drain and gate biases from varactors, large dc blocking capacitors are connected on each varactor. Control biases are applied to the center node of varactors (C_1, C_2), which are virtual grounds.

Drain and gate dc-biases are separately controlled to have feedback signals bias-level shifted. It has been known that $1/f$ noise can be reduced by lowering gate to source voltage (v_{gs}) of switching pair (Q_1, Q_2) at off state [3]. Since drain and gate biases are connected together in a conventional n-MOS VCO, it cannot make use of this effect. However, in the proposed VCO, by using the bias level shifting, v_{gs} of switching pair at off state can be brought down to less 0 V. The simulated results show that this feedback-level shifting causes 10 dB phase noise improvement and are verified by experiments.

In order to generate I-Q signals, two VCOs are coupled through series-connected transistors (Q_3, Q_4), which modulate currents of negative resistance cells (Q_1, Q_2). This direct current modulation requires less current and gives less phase mismatch and about 6 dB lower phase noise than conventional parallel-connected ones [4]. Fig. 1(c) shows connections of two VCOs to create I-Q signals. The direct connection from VCO_1 to VCO_2 and the cross connection from VCO_2 to VCO_1 make two identical VCOs operate with phase difference of 90°.

Standard 0.18 μ m TSMC foundry is used to implement the VCO, which provides five layers of Al metals and 2 μ m thick top AlCu metal. Octagonal-shape transformers are implemented with top metal layer and four and five layers for interconnections. Optimizations of the number of gate finger and length in n-MOS are performed to obtain low noise characteristics using Agilent ADS as well as the circuit design. Fig. 2 shows the photograph of a fabricated VCO. The chip size is 900×750 μm^2 including bonding pads. The layout was made as symmetrical and compact as possible to ensure differential operation and reduce parasitic inductances or capacitances.

III. Experiment Results

The test of VCOs was carried out with on-wafer probes. The output spectrums and the phase noises were obtained using HP8764E spectrum analyzer and its phase noise measurement kit. Fig. 3 shows the output spectrum at the center frequency of the VCO. The output power is about -8 dBm from 3 V supply. Fig. 4 shows phase noises across offset frequencies from 100 kHz to 1 MHz at the center frequency with the control voltage of 0.3 V. The phase noise performances (single sideband carrier to noise ratio) (SSCR) are -110 and -117 dBc/ Hz at 600 kHz and 1 MHz offset, respectively, which is more than 10 dB lower than that of previously reported quadrature VCOs in frequency range between 5 and 12 GHz as listed in Table I. The tuning range is 250 MHz from 8.08 to 7.83 GHz with the control voltage from 0 to 1 V. At the lowest control voltage, the phase noise is -109 dBc/ Hz and at the highest control voltage, -118 dBc/ Hz. Figure of merits that is used to

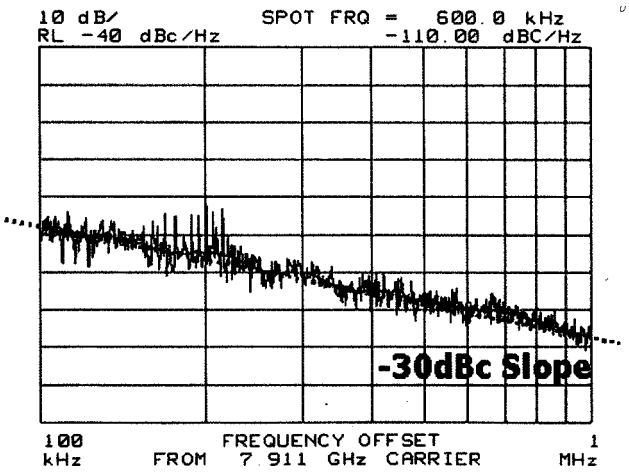

Fig. 4. Phase noise at offset frequencies from 100 kHz to 1 MHz at the center frequency ($V_d = 3$ V, $V_g = 2$ V and $V_{ctrl} = 0.3$ V).

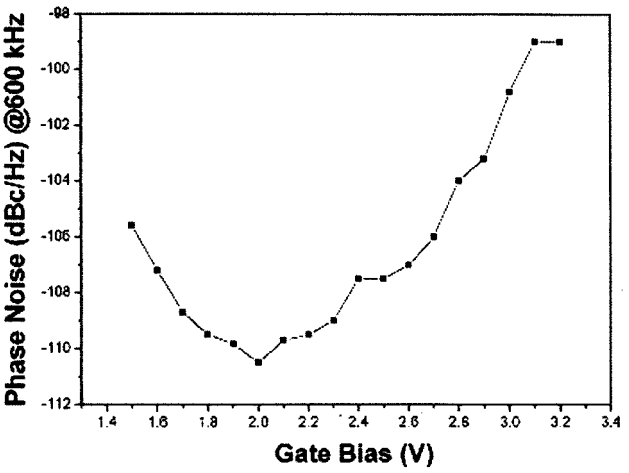

Fig. 5. Phase noise at an offset frequency of 600 kHz with V_g from 1.4 V to 3.2 V ($V_d = 3$ V and $V_{ctrl} = 1$ V).

compare the performances of oscillators also shows the lowest value of -181 dBc/ Hz. When the supply bias goes down to 2.5 V, the SSCR decreases less than 2 dB, across all offset frequencies. The phase noise curve shows -30 dB/ decade slopes across the offset frequency range. This shows that the phase noise originating from $1/$ f noise up-conversion is dominant up to 1 MHz. This high $1/f^3$ phase noise corner frequency comes from intrinsic asymmetry in quadrature VCO because the outputs of two VCOs modulate each other with 90-phase difference. Fig. 5 shows the phase noise performance as a function of gate voltages from 1.5 to 3.2 V. There is the optimum gate bias for low phase noise. At 1.4 V, the VCO starts oscillating. As the gate bias increases, the tank voltage also increases, resulting in phase noise improvement of Region I. Around the gate bias of 2 V, the tank voltage at off state goes to less than 0 V, which means the deep turn-off of the switching pair (Q1, Q2). This causes the reduction of $1/f$ noise, as a result, phase noise decreases. In region III, the tank voltage

TABLE I
COMPARISON OF VCO PERFORMANCES IN 5–12 GHZ-BAND

Performance / Parameters	Dual Band VCO	
	Low Band	High Band
Supply Voltage	4 V	
Current Consumption		
- Differential Mode	3.5 (Core), 4 mA(Buffer)/per side	
- Common Mode	8 mA /per side	
Chip size	1×1 mm^2	
Frequency (GHz)	13.2 ~ 13.8	21.8 ~ 22.2
Output Power(dBm)	2	-1
Phase Noise @ 1 MHz	-108 dBc/Hz	-106 dBc/Hz
Swithing time(ns)	4 (H →L)	24 (L →H)
F.O.M (dBc/Hz)	-176	-175

at off state increases more than V_T. Therefore active device noises increase, resulting in degradation of the phase noise performance. This bias level shifting of tank voltage improves more than 10 dB phase noise performance in simulation as well as experiment, as compared to the case of direct connection of gate and drain bias to 3 V or 2.5 V supply.

IV. CONCLUSION

We presented a fully integrated quadrature VCO at 8 GHz. The VCO are successfully realized using transformer-based LC-tank at 8 GHz in 0.18 μm CMOS technology. The low noise performance is obtained by using a transformer-based resonator and the deep turn-off-switching. The VCO uses the drain to gate feedback configuration, in which the gate bias is optimized to turn off transistor deeply, resulting in low phase noise. This gate bias optimization makes phase noise decrease more than 10 dB. To generate I-Q signal, direct current modulation is used. The VCO shows 250 MHz tuning range and the phase noise performances are -110 and -117 dBc/ Hz at 600 kHz and 1 MHz offset frequencies, respectively.

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